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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/649,672 | 08/28/2003 | Koji Okada | 100698-00014 | 5676 |

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ARENT FOX KINTNER PLOTKIN & KAHN, PLLC
Suite 400
1050 Connecticut Avenue, N.W.
Washington, DC 20036-5339

| EXAMINER | |
|---|---|
| SHINGLETON, MICHAEL B | |
| ART UNIT | PAPER NUMBER |
| 2817 | |

DATE MAILED: 10/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H/A

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/649,672 | OKADA, KOJI | |
| | Examiner | Art Unit | |
| | Michael B. Shingleton | 2817 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *21 July 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-8 and 12-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 12-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 4-6, 8, 19 and 20 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Sha et al. 6,404,294 (Sha).

Figures 7, 12 and 16, and the relevant text of Sha discloses a pll spread spectrum clock generator and method (See column 6, lines 15-25) having a phase comparator 202 that compares the reference clock signal (Sometimes referred to by applicant as a "standard clock signal".) to clock signal that is feedback (Sometimes referred to by applicant as an "operating clock signal".). Element 100 is a voltage controlled oscillator i.e. VCO that generates the signal that fed back to the phase comparator. The VCO of Sha has a V to I converter 112 that does the conversion of a voltage to a current. Element 110 is part of a variable current circuit that provides a fluctuating current signal "ILOAD". Note that the division ratio is changed to spread the spectrum this in turn causes the voltage input to the VCO to vary and since the control signal 104 that causes the current to vary is varied and this will cause a different current at the output of the V to I converter and thus these changes will cause a change in the voltage at the input of the VCO which will result in a further change in these current signals as well as the final output frequency because of the feedback path. This forms part of the first circuit that generates a plurality of current signals by changing the current signals. This also forms part of variable current circuit and the circuitry 210 of Sha forms part of the control circuit that controls the variable current circuit. The internal circuitry to the divider determines the range of change of frequency of the clock for divider has a finite range of division. As recognized by Sha in column 4, around line 19 the signal output from the VCO is dependent at least in part on the changing current signals ILOAD. Thus the VCO like that of applicant also has a current controlled oscillator component. Note that the internal circuitry of the VCO of Sha forms the "second and third" circuits of claims like claim 9 for a plurality of current signals are generated, i.e. at least first and second current signals are generated. When the first current signal ILOAD is generated this as noted above causes a first clock signal or "operating clock signal" to be generated based on this signal. When

the second current signal ILOAD is generated this as noted above causes a second clock signal or "operating clock signal" to be generated based on this signal. Note that the charge pump 204 clearly supplies an output signal based on the comparison made by the phase comparator in Sha. The VCO of Sha also is responsive to this charge pump as is clearly illustrated by Sha. Note that element 110' also forms a current D/A converter in that the digital signal is converted into an analog current signal ILOAD and is part of the variable current circuit. With respect to claims like claims 9, The phase comparator clearly outputs a result based upon the standard clock signal and the comparison clock (feedback) signal. The charge pump 204 generates a current based on this comparison and the filter 206 is part of a "third circuit"(claim 9) that generates a second frequency clock signal based on the current signal from the charge pump. A first circuit is formed at least in part by the input 104 that is also based on the result of the comparison (See Figure 16) and this cases changes in the ILOAD current (the second current signal) which as noted above causes changes in the output frequency, i.e. generates a second frequency clock. As noted above the ILOAD currents are varied which varies the current output of the V-to-I converter which causes the second frequency to be generated, i.e. a second clock is formed.

Claims 12 and 14-18 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Takla 5,978,425 (Takla) or record.

Figure 2 and the relevant text of Takla discloses a clock circuit having the pll or first clock generator composed of elements 218, 222, 246, 250 254 and 234. This pll clearly has a phase comparator that compares the reference or standard clock and the operating clock. Element 254 is a V-to-I converter that outputs a current to the current controlled oscillator 234 based on the above comparison. A first clock signal is generated by this loop. A second clock signal is generated by the loop that consists of elements 227, 229 and 230. Element 230 is a D/A converter that converts the current control signal to a variable current signals that are applied to the current controlled oscillator 224 and thus forms a second clock generator circuit. Element 234 also forms a second current controlled oscillator for the second clock generator. The variable current signals clearly causes changes in the oscillation frequency of element 234. The top of column 6 of Takla clearly recites the range of variable current which sets forth a set range of frequency changes.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at

the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2, 3 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sha et al. 6,404,294 (Sha) in view of Applicant's Admitted prior art as represented by Figure 1 (AAPA)

Sha lacks the use of a divider connected between the reference clock source and the phase comparator. Such is commonly provided for so as to allow for a higher frequency reference clock to be used with the phase comparator and to allow for the reference clock to be selected or varied dependent on the selection of the division ratio. AAPA gives one example of this.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to utilized a divider connected between the reference clock source and the phase comparator of Sha so as to allow the use of a higher frequency reference clock and to allow for the adjustment or selection of the reference frequency applied to the phase comparator as is clearly evident and taught by AAPA.

The current D/A converter of Sha fails to show the use of a low pass filter. However, current D/A converters that employ a low pass filter are one art recognized equivalent forms of current D/A converter. Note that applicant's amendment necessitates the new rejection. Accordingly it would have been obvious to one of ordinary skill in the art at the time the invention was made to replace the current D/A converter of Sha with one that includes a low pass filter since the examiner takes Official Notice of the equivalence of the current D/A converter with low pass filter and the current D/A converter of Sha for their use in the electronic circuitry art and the selection of any of these known equivalents to provide a D/A function would be within the level of ordinary skill in the art. In fact note that original claims 3 and 7 were both in a Markush format wherein the elements of the alternative are seen as equivalents.

Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takla 5,978,425 (Takla) or record.

The reasoning as applied to claims 12 and 14-18 above and the following: Takla is silent on the details current D/A converter 230. In particular the current D/A converter of Takla fails to show the use of a low pass filter. However, current D/A converters that employ a low pass filter are one art recognized equivalent forms of current D/A converter. Note that applicant's amendment necessitates the new rejection.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to replace the current D/A converter of Takla with one that includes a low pass filter because as the Takla reference is silent on the exact structure of the current D/A converter one of ordinary skill in the art would have been motivated to use any art-recognized equivalent current D/A converter

such as the conventional current D/A converter that employs a low pass filter. Note that original claim 13 was in a Markush format wherein the elements of the alternative are seen as equivalents.

Applicant's arguments filed 8-3-2005 have been fully considered but they are not persuasive. Applicant states that Sha does not or suggest a current D/A converter that is controlled by a digital signal. The previous office action clearly pointed to 110' and note that bit signals, i.e. the digital signal causes a current and thus the D/A converter of Sha is clearly a current D/A converter that is controlled by a digital signal. In fact column 5, line 28 of Sha specifically states "digital". Also note that applicant has not provided a specific definition for "current D/A converter". Applicant states that Takla "teaches a single clock". Again applicant has not provided a specific definition for clock and one normal meaning for clock is not that produces a frequency. The Office action was very specific in identifying the two clocks. One is formed by the phase locked loop but the other is formed by at least elements 227 and 230. Note that column 6 around line 64 of Takla clearly recites that frequency is increased. Just because these two clock arrangements share a common output does not distract from the fact that there are two clocks. One clock circuit is active at one time and the other is active at another time. The claims just do not recite that the clocks cannot share a common output. Also note like Sha the D/A converter of Takla operates on a digital signal and as such a current is generated and thus the D/A converter of Takla is a current D/A converter. Also note that when the second clock is active the M number of peaks is greater than N for as stated above the frequency is increased.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael B. Shingleton whose telephone number is (571) 272-1770.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal, can be reached on (571)272-1769. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306 and after July 15, 2005 the fax number will be 571-273-8300. Note that old fax number (703-872-9306) will be service until September 15, 2005.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MBS
September 23, 2005

Michael B Shingleton
Primary Examiner
Group Art Unit 2817